What is claimed is:

1. A circuit comprising:

a discrete-time FIR (Finite Impulse Response) filter comprising n multiplier units to implement a filter response $[\bar{h}(t)]_i$, $i = 0,1,\ldots,n-1$, where t is a time index, the FIR filter to filter a discrete-time sequence of input voltages $x(t)$ to provide a sequence of filtered output voltages $z(t)$ where $z(t) = \sum_{i=0}^{n-1}[\bar{h}(t)]_i x(t-i)$; and

a data generator to provide a discrete-time sequence of desired voltages $d(t),\ t = 1,2,\ldots,T$;

wherein for $t = 1,2,\ldots,T$, the filter response satisfies an update relationship $[\bar{h}(t+1)]_i = [\bar{h}(t)]_i + \mu[\mathrm{sgn}\{d(t)\} - \mathrm{sgn}\{z(t) - Kd(t)\}]\mathrm{sgn}\{x(t-i)\},\ i = 0,1,\ldots,n-1$, where μ and K are scalars and $\mathrm{sgn}\{\}$ denotes sign.

2. The circuit as set forth in claim 1, wherein each multiplier unit comprises a voltage-to-current converter and a current steering digital-to-analog converter.

3. The circuit as set forth in claim 1, wherein the voltages $x(t)$, $z(t)$, and $d(t)$ are differential voltages.

4. A circuit comprising:

a discrete-time FIR (Finite Impulse Response) to filter a discrete-time input sequence of voltages $x(t)$ where t is a discrete-time index, to provide, for $t = 1,2,\ldots,T$,

a voltage indicative of $z(t)=\sum_{i=0}^{n-1}[\bar{h}(t)]_i x(t-i)$ where $[\bar{h}(t)]_i, i=0,1,\ldots,n-1$ are n weights indexed by t;

a data generator to provide a discrete-time sequence of desired voltages $d(t), t=1,2,\ldots,T$;

a latch circuit to provide, for $t=1,2,\ldots,T$, a voltage indicative of $\operatorname{sgn}\{z(t)-Kd(t)\}$ where K is a weight and $\operatorname{sgn}\{\}$ denotes the sign function;

a digital summer to provide, for $t=1,2,\ldots,T$, n voltages indicative of $\operatorname{sgn}\{d(t)\}-\operatorname{sgn}\{z(t)-Kd(t)\}, \quad i=0,1,\ldots,n-1$;

a digital multiplier to provide, for $t=1,2,\ldots,T$, n voltages indicative of $\mu[\operatorname{sgn}\{d(t)\}-\operatorname{sgn}\{z(t)-Kd(t)\}]\operatorname{sgn}\{x(t-i)\}, i=0,1,\ldots,n-1$ where μ is a weight;

a digital summer and a delay element to provide to the FIR filter, for $t=1,2,\ldots,T$, n voltages indicative of $[\bar{h}(t)]_i+\mu[\operatorname{sgn}\{d(t)\}-\operatorname{sgn}\{z(t)-Kd(t)\}]\operatorname{sgn}\{x(t-i)\}, i=0,1,\ldots,n-1$ so that for $t=1,2,\ldots,T$ the weights $[\bar{h}(t+1)]_i, i=0,1,\ldots,n-1$ are given by $[\bar{h}(t+1)]_i=[\bar{h}(t)]_i+\mu[\operatorname{sgn}\{d(t)\}-\operatorname{sgn}\{z(t)-Kd(t)\}]\operatorname{sgn}\{x(t-i)\}, i=0,1,\ldots,n-1$.

5. The circuit as set forth in claim 4, the FIR filter comprising n multiplier units, each multiplier unit, denoted as multiplier unit(i), $i=0,1,\ldots,n-1$, each multiplier unit(i), $i=0,1,\ldots,n-1$, comprising:

a voltage-to-current converter(i) to provide as output a current $I_{VC}(i)$ indicative of the voltage $x(t-i)$; and

a current steering digital-to-analog converter(i) to shunt a portion of $I_{VC}(i)$ to provide as output at time t a current indicative of $[\bar{h}(t)]_i x(t-i)$.

6. The circuit as set forth in claim 5, further comprising:

a multiplier unit comprising:

a voltage-to-current converter to provide as output a current I_{VC} indicative of the voltage $d(t)$; and

a current steering digital-to-analog converter to shunt a portion of I_{VC} to provide as output at time t a current indicative of $Kd(t)$.

7. The circuit as set forth in claim 4, wherein the voltages $x(t)$, $z(t)$, and $d(t)$ are differential voltages.

8. A computer system comprising:

a board comprising a fist transmission line an a second transmission line; and

a receiver coupled to the first an second transmission lines, the receiver comprising:

a discrete-time FIR (Finite Impulse Response) filter comprising n multiplier units to implement a filter response $[\bar{h}(t)]_i$, $i = 0,1,\ldots,n-1$, where t is a time index, the FIR filter to filter a discrete-time sequence of input voltages $x(t)$ to provide a sequence of filtered output voltages $z(t)$ where $z(t) = \sum_{i=0}^{n-1}[\bar{h}(t)]_i x(t-i)$; and

a data generator to provide a discrete-time sequence of desired voltages $d(t),\ t = 1,2,\ldots,T$;

wherein for $t = 1,2,\ldots,T$, the filter response satisfies an update relationship

$$[\bar{h}(t+1)]_i = [\bar{h}(t)]_i + \mu[\mathrm{sgn}\{d(t)\} - \mathrm{sgn}\{z(t) - Kd(t)\}]\mathrm{sgn}\{x(t-i)\},\ i = 0,1,\ldots,n-1,$$

where μ and K are scalars and $\mathrm{sgn}\{\}$ denotes sign.

9. The computer system as set forth in claim 8, wherein each multiplier unit comprises a voltage-to-current converter and a current steering digital-to-analog converter.

10. The computer system as set forth in claim 8, wherein the voltages $x(t)$, $z(t)$, and $d(t)$ are differential voltages.